Code No: B5506, B5703 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II Semester Examinations, October/November 2011
LOW POWER VLSI DESIGN
(COMMON TO EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) What are the difference problems associated with Low Power VLSI Design? Discuss.
b) Explain about SOI Technology. [12]

2.a) Draw the structure for optimized twin – Well BI CMOS structure with self aligned p and n^+ buried layers for improved packing density and explain about the same.
b) Explain about punch through in short – channel MUSFETS. [12]

3.a) With the help of neat sketches explain about Polysizicon Emitter High-performance BICMOS structures and explain about the process steps.
b) What are the steps in implementing copper metallization in deep sub micros process? Explain. [12]

4.a) Give the 0.2 μ in SOI BICMOS process flow with sketches and explain the same.
b) Using necessary equations, explain about the properties of fully depleted SOI MOSFETS. [12]

5.a) Explain about MOS structure capacitances, using necessary equations.
b) Explain about LEVEL 3 Model MOSFETS. [12]

6.a) Explain about EKV MOSFET model with the help of a circuit diagram.
b) Explain the sub micron CMOS Technology. [12]

7.a) Draw the circuit for FS–CMBL two in put NAND gate with positive feedback and explain the same.
b) Draw a logic circuit in BICMOS configuration using lateral parasitic pnp BJT in a PMOS. Structure BIFET and explain its working. [12]

8. Write notes on any Two
a) ESD – free BICMOS circuits
b) Full Swing Multi Drain / Multi Collector complimentary BICMOS buffers
c) Gummel - Poon Model of MOSFETS. [12]

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